REMARKS

Reconsideration and allowance is respectfully requested. Before entry of this Response, claims 1-23 were pending. In the Office Action, claims 1-23 were rejected. In the present Response, no claims are amended. After entry of the Response, claims 1-23 are pending.

I. Claims 1-5, 7, 9-19 and 21-23

Claims 1-5, 7, 9-19 and 21-23 are rejected under 35 U.S.C. § 102(b) as being anticipated by Bongiorno et al. (U.S. Pat. 6,292,045 B1) (Office Action, p. 2, lines 22-23).

A. Independent claim 1

Bongiorno does not form the basis for a valid rejection of claim 1 under § 102(b) because Bongiorno does not disclose either (i) coupling one clock circuit after decoupling another clock circuit, or (ii) enabling a clock circuit.

(i) Bongiorno does not disclose coupling one clock after decoupling another clock.

Claim 1 recites "(b) decoupling the first clock circuit . . . (c) coupling a second clock circuit . . . (e) decoupling the second clock circuit . . . and (f) coupling the third clock circuit . . .". In the Office Action, the Examiner argues:

> "Bongiorno shows a table (Table 1, column 6) that represents in what order the clock sources can be selected. If code '000' is coded, then the first clock selected will be clock source 10. If clock source 10 were to fail, the next selected clock source would be clock 20. And, if clock source 20 were to fail, the next selected clock source would be clock 30 (column 6, lines 1-35). The clock selection process of coupling and decoupling is stepped out in Fig. 4 at steps 400-440 (column 7, lines 38-57). Therefore, Bongiorno ***does teach*** coupling a third clock circuit after decoupling a second clock circuit after coupling the second clock circuit after decoupling a first clock circuit." (Office Action, p. 11, line 22 – p. 12, line 7).

Applicants respectfully disagree. The Examiner's argument mischaracterizes the disclosure of Bongiorno. Bongiorno does not disclose coupling more than one clock signal. Bongiorno does not disclose, as the Examiner suggests, coupling clock source 10, and then coupling clock source 20 if clock source 10 were to fail. It is clear from the disclosure of Bongiorno quoted below that Bongiorno discloses only a "priority scheme" for coupling a single clock (admittedly chosen from among multiple available clocks). Bongiorno discloses that where a first priority clock 10 is unavailable, a second selected clock can be either 20 or 30, but not 20 and then 30 as the Examiner asserts. Bongiorno explains:

> "FIG. 3A illustrates a second preferred embodiment of a present inventive circuit 200. Instead of only one detector, the circuit 200 includes three detectors 51, 52 and 53 for three clock sources 10, 20 and 30, respectively. . . . The clock signal selector receives a programmed code that designates which clock signal should be selected. If the designated clock signal is available, the clock signal selector 600 generates a first control signal and provides it to the switching means that in response outputs the selected, designated clock signal to the timer 70. If the designated clock signal is not available, the clock signal selector 600 automatically selects one of the undesignated clock signals that have been received and thus are available. Based on this selection, the clock signal selector generates a second control signal and provides it to the switching means that in response outputs the selected, undesignated clock signal to the timer 70." (Bongiorno, col. 5, lines 29-52) (emphasis added)
>
> "It should be noted that the circuits 100 and 200 may be modified to detect and select two clock sources or more than three clock sources. As the number of available clock sources increases, the probability that a watchdog timer or a microprocessor will not operate decreases exponentially. Furthermore, in addition to designating a clock signal from a specific clock source for a clock source selector to select, the programmed code may also instruct the clock signal selector to choose the undesignated clock signals based on priority and their availability when the designated clock signal is unavailable and when the undesignated clock signals are available." (Bongiorno, col. 5, line 58 – col. 6, line 2) (emphasis added)
>
> "Table 1 illustrates this priority scheme with respect to the three clock sources 10, 20 and 30. Table 1 shows an example of how the programmed code may be used to selectively select the clock sources

> 10, 20 and 30 based on priority. Two examples of how the clock signal selector of FIG. 1A functions based on the received programmed codes "000" and "011" are as follows.
> First, if the instruction register of the clock signal selector receives the programmed code "000", the decoder of the clock signal selector would decode this programmed code so that the clock signal selector would select the clock signal from the clock source 10 when the clock source 10 is available regardless of whether the clock sources 20 and 30 are available or not. If the clock source 10 is not available, the clock signal selector would select the clock source 20 when the clock source 20 is available regardless of whether the clock source 30 is available or not. Only when both the clock sources 10 and 20 are not available, the clock signal selector would select the clock source 30." (Bongiorno, col. 6, lines 16-34)

Thus, the Examiner's statement, "If code '000' is coded, then the first clock selected will be clock source 10. If clock source 10 were to fail, the next selected clock source would be clock 20," mischaracterizes Bongiorno's disclosure at lines 23-34 of column 6 to the extent that "the next selected" clock is construed to mean "the next coupled" clock. And to the extent that the next selected clock of Bongiorno is not coupled, the disclosure of Bongiorno does not disclose the limitations of claim 1.

The Examiner also states that the "clock selection process of coupling and decoupling is stepped out in Fig. 4 at steps 400-440 (column 7, lines 38-57)" (Office Action, p. 12, lines 4-5). The steps of figure 4, however, do not disclose coupling and decoupling. Instead, step 410 of figure 4 states, "Programming an integrated circuit to choose one of the first and second clock signals" (emphasis added). Moreover, step 430 discloses that either the designated clock signal or the undesignated clock signal is selected, but not one and then the other. Bongiorno explains:

> "FIG. 4 illustrates the present inventive steps of a method for detecting and selecting one of clock signals of at least two clock sources and providing the selected clock signal to a device of an integrated circuit that requires a clock signal in order to operate. . . . Note that more than two clock sources may be provided in order to increase the probability that the device is constantly working. In step 410, the

> integrated circuit is programmed to choose one of the first and second clock signals designated by a programmed code. . . . In step 430, the designated clock signal is selected when it is available, and the undesignated clock signal is selected when the designated clock signal is unavailable and when the undesignated clock signal is available. In step 440, the selected clock signal is provided to the device. Such device may be a watchdog timer or a microprocessor of the integrated circuit." (Bongiorno, col. 7, lines 16-34)

The passage of Bongiorno cited by the Examiner (column 7, lines 38-57) discloses that only one selected clock is provided to the device. Thus, the priority scheme of Bongiorno for selecting a clock source does not disclose coupling a third clock circuit after decoupling a second clock circuit after coupling the second clock circuit after decoupling a first clock circuit.

(ii) Bongiorno does not disclose enabling a clock circuit.

Claim 1 recites, "(d) enabling a third clock circuit after the coupling in (c)". In the Office action dated May 16, 2006, the Examiner admits that "Bongiorno fails to disclose the method comprising the step: (d) enabling a third clock circuit" (5/16/06 Office action, p. 4, lines 14-15). Again in the Office action dated September 28, 2006, the Examiner admits that "Bongiorno fails to disclose the method comprising the step: (d) enabling a third clock circuit" (9/28/06 Office action, p. 5, lines 3-4). Yet again in the Office action dated December 27, 2006, the Examiner admits that "Bongiorno fails to disclose the method comprising the step: (d) enabling a third clock circuit." (12/27/06 Office action, p. 4, lines 1-2). Although the Examiner now claims that Bongiorno discloses "(d) enabling a third clock circuit (30) after the coupling in (c)" (Office Action, p. 3, lines 6-7), the Examiner's admissions in the Office actions of May 16, September 28 and December 27, 2006, remain correct.

The Examiner now states that "Bongiorno does teach selecting/coupling/enabling a third clock source (30) wherein said third clock source is selected using a switching means (66 or 660) that inherently couples

and enables the selected clock source (column 4, lines 61 thru column 5, line 7 and column 5, lines 29-52)" (Office Action, p. 12, lines 12-15) (emphasis added). The Examiner's argument is inadequate for three reasons.

First, it is improper to construe the separate claim terms "coupling" and "enabling" to be equivalent. Claim 1 recites both "enabling a third clock circuit" and "coupling the third clock circuit". The tenets of claim differentiation require that the separate claim limitations "enabling" and "coupling" be interpreted differently. These claim limitations cannot be disclosed by the same teaching of Bongiorno. A claim interpretation that construes the separate claim terms "coupling" and "enabling" to be equivalent would be presumptively unreasonable. See, e.g., *Karlin Tech. Inc. v. Surgical Dynamics Inc.*, 177 F.3d 968, 50 USPQ2d 1465, 1468 (Fed. Cir. 1999).

Second, the passages of Bongiorno cited by the Examiner do not disclose that clock source (30) is enabled using switching means (66 or 660). To the contrary, the cited passages of Bongiorno state that switching means 66 receives clock sources 10, 20 and 30 as well as a control signal "[b]ased on the received clock source availability signal" (Bongiorno, col. 4, line 67 – col. 5, line 1). Thus, switching means (66 or 660) outputs clock source (30) only if the clock source availability signal indicates that clock source (30) is already available. Bongiorno does not disclose that clock source (30) is enabled.

Third, switching means (66 or 660) does not inherently enable clock source (30). To the extent the Examiner is arguing that switching means 66 inherently enables clock source (30), the Examiner is asked to present extrinsic evidence of this fact. "To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991)" Metabolite Labs., Inc. v. Lab. Corp. of Am. Holdings, 370 F.3d 1354, 1367 (Fed. Cir. 2004) (emphasis

added). The ability of a switching means to enable a clock source is not an inherent characteristic of a switching means. The Examiner has not established a *prima facie* case of anticipation because Bongiorno does not disclose this ability, and the Examiner has provided no extrinsic evidence teaching that the ability is necessarily present in the circuit of Bongiorno. For example, switching means 66 could switch a clock from clock source (30) where clock source (30) is always on. Indeed, Bongiorno does not mention any of "enabling", "turning on", "starting" or "powering" a clock signal. The clock sources selected in Bongiorno are already either "available" or "unavailable". Thus, Bongiorno does not disclose, as the Examiner asserts, that clock circuit (30) is enabled after clock circuit (20) is coupled to the system clock input lead of processor (80). Clock circuit (30) is already either "available" or "unavailable" when the priority scheme described by programmed code "000" is applied.

(iii) Grounds for non-allowability stated in the Advisory Action have been removed.

In the Advisory Action dated March 14, 2007, the Examiner stated that the amendment dated February 27, 2007, did not place claim 1 in a condition for allowance because "claim 1 does not have the limitation that the steps be carried out in any particular order. Therefore, the Applicant's arguments are not persuasive." (Advisory Action, p. 2, lines 1-6) The Examiner's statements suggest that claim 1 would be allowable if claim 1 requires that the steps be carried out in a particular order. The amendment dated March 27, 2007, amended claim 1 to recite that the steps are carried out in a particular order. In the Office Action, the Examiner does not retract the reason why the amendment dated February 27, 2007, did not place claim 1 in a condition for allowance. Because this reason has been removed, claim 1 is allowable.

Therefore, Bongiorno does not disclose either (i) coupling one clock circuit after decoupling another clock circuit, or (ii) enabling a clock circuit. Moreover,

the reasons for non-allowability of claim 1 have been removed. Reconsideration of the § 102(b) rejection and allowance of claim 1 are requested.

B. Dependent claims 2-5, 7, 9-10 and 22-23

Claims 2-5, 7, 9-10 and 22-23 depend from claim 1 and are allowable for at least the same reasons for which claim 1 is allowable. Reconsideration of the § 102(b) rejection and allowance of claims 2-5, 7, 9-10 and 22-23 are requested.

C. Independent claim 11

Claim 11 recites a "terminal coupled to a first clock circuit . . . the clock controller is adapted to decouple the system clock input lead from the terminal and to couple the system clock input lead to the second clock circuit upon detecting that the first clock signal has failed, and wherein the clock controller is further adapted to turn on the third clock circuit upon detecting that the first clock signal has failed" (emphasis added).

Bongiorno does not form the basis for a valid rejection of claim 11 under § 102(b) because Bongiorno does not disclose either (i) decoupling a first clock and coupling a second clock upon detecting that the first clock has failed, or (ii) turning on a clock circuit.

(i) Bongiorno does not disclose coupling one clock and decoupling another clock after detecting that the other clock has failed.

The Examiner states that the controller 40 of Bongiorno "is adapted to decouple (via 66) the system clock input lead from the terminal and to couple the system clock input lead to the second clock circuit upon detecting that the first clock signal has failed, and wherein the clock controller is further adapted to turn on the third clock circuit upon detecting that the first clock signal has failed (column 2, lines 41-62 and column 3, line 52 thru column 4, line 60 and column 4, line 61 thru column 5, line 28 and column 5, line 53 thru column 6, line 35 and column 7, line 45-57; Figs. 1B and 3A)" (Office Action, p. 5, lines 15-21)

(emphasis added). Thus, the Examiner cites the same passages of Bongiorno as he cites with regard to claim 1.

As explained above with regard to claim 1, Bongiorno does not disclose coupling one clock after decoupling another. Bongiorno does not disclose, as the Examiner suggests, decoupling clock source 10 and coupling clock source 20 upon detecting that clock source 10 has failed. Bongiorno discloses only a "priority scheme" for coupling a single clock and does not disclose decoupling one clock and then coupling another. Bongiorno discloses that where a first priority clock 10 is unavailable, a second selected clock can be either 20 or 30. But Bongiorno does not disclose that where first clock 10 is coupled that it is ever later decoupled. Bongiorno discloses that if first clock 10 is not available, it is simply not selected. Bongiorno explains:

> "The clock signal selector receives a programmed code that designates which clock signal should be selected. If the designated clock signal is available, the clock signal selector 600 generates a first control signal and provides it to the switching means that in response outputs the selected, designated clock signal to the timer 70. If the designated clock signal is not available, the clock signal selector 600 automatically selects one of the undesignated clock signals that have been received and thus are available. Based on this selection, the clock signal selector generates a second control signal and provides it to the switching means that in response outputs the selected, undesignated clock signal to the timer 70." (Bongiorno, col. 5, lines 40-52) (emphasis added)
>
> "[I]n addition to designating a clock signal from a specific clock source for a clock source selector to select, the programmed code may also instruct the clock signal selector to choose the undesignated clock signals based on priority and their availability when the designated clock signal is unavailable and when the undesignated clock signals are available." (Bongiorno, col. 5, line 63 – col. 6, line 2) (emphasis added)
>
> "First, if the instruction register of the clock signal selector receives the programmed code "000", the decoder of the clock signal selector would decode this programmed code so that the clock signal selector would select the clock signal from the clock source 10 when the clock source 10 is available regardless of whether the clock sources 20 and

> 30 are available or not. If the clock source 10 is not available, the clock signal selector would select the clock source 20 when the clock source 20 is available regardless of whether the clock source 30 is available or not. Only when both the clock sources 10 and 20 are not available, the clock signal selector would select the clock source 30." (Bongiorno, col. 6, lines 23-34)

Thus, the Examiner's statement that Bongiorno discloses controller 40 adapted to decouple first clock 10 and to couple second clock 20 upon detecting that first clock 10 has failed is not supported by the passages cited by the Examiner. Bongiorno never mentions decoupling first clock 10.

(ii) Bongiorno does not disclose turning on a clock circuit.

In the Office action dated May 16, 2006, the Examiner admits that "Bongiorno fails to disclose the clock controller is adapted to turn on the third clock circuit" (5/16/06 Office action, p. 8, lines 9-10). Again in the Office action dated September 28, 2006, the Examiner admits that "Bongiorno fails to disclose the clock controller is adapted to turn on the third clock circuit" (9/28/06 Office action, p. 9, lines 1-2). Yet again in the Office action dated December 27, 2006, the Examiner admits that "Bongiorno fails to explicitly disclose the clock controller is further adapted to turn on the third clock circuit upon detection that the first clock signal has failed." (12/27/06 Office action, p. 8, lines 1-2). Even in the Advisory Action dated March 14, 2007, the Examiner states:

> "In re independent claim 11, Applicant argues that "...neither Bongiorno nor the Lichter provisional application teaches a clock controller adapted to turn on a replacement clock circuit upon detecting that the primary clock has failed..." (REMARKS, page 11). However, this limitation is taught in Lichter such that a switch selects a functional redundant clock when 'power is established' to the working and in tolerance clock (column 3, lines 19-31). Therefore, the Applicant's arguments are not persuasive." (Advisory Action, p. 2, lines 7-10) (emphasis added)

Although the Examiner now claims that the controller 40 of Bongiorno "is further adapted to turn on the third clock circuit upon detecting that the first clock signal

has failed" (Office Action, p. 5, lines 17-19) (emphasis added), the Examiner's admissions in the Office actions of May 16, September 28 and December 27, 2006, remain correct.

The passages of Bongiorno cited by the Examiner do not disclose that clock source (30) is turned on. To the contrary, the cited passages of Bongiorno state that switching means 66 receives clock source 30 as well as a control signal "[b]ased on the received clock source availability signal" (Bongiorno, col. 4, line 67 – col. 5, line 1). Switching means 66 outputs clock source (30) only if the clock source availability signal indicates that clock source (30) is already available; Bongiorno does not mention any of "turning on", "enabling", "starting" or "powering" a clock signal. The clock sources selected in Bongiorno are already either "available" or "unavailable", and Bongiorno does not disclose that any of the clock sources is turned on.

Therefore, Bongiorno does not disclose either (i) decoupling the first clock source and coupling the second clock source upon detecting that the first clock source has failed, or (ii) turning on the third clock source. Reconsideration of the § 102(b) rejection and allowance of claim 11 are requested.

D. Dependent claims 12-18

Claims 12-18 depend directly or indirectly from claim 11 and are allowable for at least the same reasons for which claim 11 is allowable. Reconsideration of the § 102(b) rejection and allowance of claims 12-18 are requested.

E. Independent claim 19

Claim 19 recites, "means for . . . decoupling the terminal from the system clock input lead and coupling the second clock circuit to the system clock input lead . . ., wherein the means turns on the third clock circuit upon detecting that the first clock signal is inadequate" (emphasis added).

As explained above with regard to claim 11, Bongiorno also does not form the basis for a valid rejection of claim 19 because Bongiorno does not disclose

either (i) decoupling a first clock and coupling a second clock upon detecting that the first clock has failed, or (ii) turning on a clock circuit.

(i) Bongiorno does not disclose coupling one clock and decoupling another clock upon detecting that the other clock is inadequate.

The Examiner states that Bongiorno discloses a means "for decoupling (via 66) the terminal from the system clock input lead and coupling the second clock circuit to the system clock input lead, . . . wherein the means turns on the third clock circuit upon detecting that the first clock signal is inadequate (column 2, lines 41-62 and column 3, line 52 thru column 4, line 60 and column 4, line 61 thru column 5, line 28 and column 5, line 53 thru column 6, line 35 and column 7, line 45-57; Figs. 1B and 3A)" (Office Action, p. 5, lines 15-21) (emphasis added). Thus, the Examiner cites the same passages of Bongiorno as he cites with regard to claims 1 and 11.

As explained above with regard to claims 1 and 11, Bongiorno does not disclose coupling one clock after decoupling another. Bongiorno does not disclose, as the Examiner suggests, decoupling clock source 10 and coupling clock source 20 upon detecting that clock source 10 is inadequate. Bongiorno discloses only a "priority scheme" for coupling a single clock and does not disclose decoupling one clock and then coupling another. Bongiorno discloses that where a first priority clock 10 is unavailable, a second selected clock can be either 20 or 30. But Bongiorno does not disclose that where first clock 10 is coupled that it is ever later decoupled. Bongiorno discloses that if first clock 10 is not available, it is simply not selected.

Thus, the Examiner's statement that Bongiorno discloses a means for detecting (40) and for decoupling (66) first clock 10 and coupling second clock 20 upon detecting that first clock 10 is inadequate is not supported by the passages cited by the Examiner. Bongiorno never mentions decoupling first clock 10.

(ii) Bongiorno does not disclose a means for turning on a clock circuit.

The passages of Bongiorno cited by the Examiner do not disclose that clock source (30) is turned on. To the contrary, the cited passages of Bongiorno state that switching means 66 receives clock source 30 as well as a control signal "[b]ased on the received clock source availability signal" (Bongiorno, col. 4, line 67 – col. 5, line 1). Switching means 66 outputs clock source (30) only if the clock source availability signal indicates that clock source (30) is already available; Bongiorno does not mention any of "turning on", "enabling", "starting" or "powering" a clock signal. The clock sources selected in Bongiorno are already either "available" or "unavailable", and Bongiorno does not disclose that any of the clock sources is turned on.

Therefore, Bongiorno does not disclose either (i) a means for decoupling a first clock source and coupling a second clock source upon detecting that the first clock source is inadequate, or (ii) a means that turns on a third clock source. Reconsideration of the § 102(b) rejection and allowance of claim 19 are requested.

F. Dependent claim 21

Claim 21 depends from claim 19 and is allowable for at least the same reasons for which claim 19 is allowable. Reconsideration of the § 102(b) rejection and allowance of claim 21 is requested.

II. Dependent claim 6

Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Bongiorno in view of Lichter et al. (U.S. Pat. 6,970,045 B1) (Office Action, p. 9, lines 10-12). The combination of Bongiorno and Lichter does not form the basis for a valid rejection of claim 6 under § 103(a) because the combination of Bongiorno and Lichter does not teach at least two limitations of base claim 1.

Claim 6 includes the following limitation of base claim 1: "(b) decoupling the first clock circuit . . . (c) coupling a second clock circuit . . . (e) decoupling the

second clock circuit . . . and (f) coupling the third clock circuit . . ." As explained above with regard to claim 1, Bongiorno does not teach coupling a third clock circuit after decoupling a second clock circuit after coupling the second clock circuit after decoupling a first clock circuit. Lichter also does not teach coupling one clock circuit after decoupling another clock circuit.

Claim 6 also includes the following limitation of base claim 1: "(d) enabling a third clock circuit after the coupling in (c)". Bongiorno does not teach enabling a clock circuit as explained above with regard to claim 1. The passages of Bongiorno cited by the Examiner do not disclose that clock source (30) is enabled using switching means (66). To the contrary, the cited passages of Bongiorno teach that switching means (66) outputs clock source (30) only if clock source (30) is already available. Thus, switching means (66) couples clock source (30) to processor 80 only if clock source (30) is already available, and Bongiorno does not teach that clock source (30) is enabled.

Claim 6 recites, "wherein the third clock circuit is enabled in (d) by powering up the third clock circuit". The Lichter provisional application 60/482,557 does not teach powering up a clock circuit. Moreover, teachings in the Lichter Patent 6,970,045 may not be used as prior art to render claim 6 unpatentable to the extent that those teachings are not included in the Lichter provisional application 60/482,557. The Examiner states:

> "Applicant also argues that reference Lichter does not have priority over the instant application's effective filing date. However, filing a provisional application under 35 USC § 119(e) deems the reference [Lichter] to have an earlier effective filing date than said instant application. The Applicant is instructed to refer to MPEP 706.02 for further detail." (Office Action, p. 12, lines 16-19)

The Examiner's statement above incorrectly applies 35 USC § 119(e) and MPEP 706.02 in this instance. MPEP 2136.03(III) is instructive.* Although the Lichter

* "PRIORITY FROM PROVISIONAL APPLICATION UNDER 35 U.S.C. 119(e): The 35 U.S.C. 102(e) critical reference date of a U.S. patent or U.S. application publications and certain international application publications entitled to the benefit of the filing date of a provisional

Patent 6,970,045 does claim priority to a provisional application 60/482,557 filed on June 25, 2003, before the present application, the teachings of the Lichter Patent 6,970,045 may not be applied against the instant application to the extent that those teachings first appear in a patent document filed after the instant application was filed. The Examiner has not rebutted Applicants' previous statement that the sparse disclosure of provisional application 60/482,557 does not teach powering up a clock circuit. A provisional application does not reserve an earlier filing date for new subject matter first disclosed in a non-provisional application that claims priority to the provisional application. Teachings that first appear in the disclosure of the Lichter Patent 6,970,045 (as opposed to the Lichter provisional application 60/482,557) may not properly be cited as prior art against the present application 10/764,391 because Lichter was filed on February 19, 2004, which was after the present application 10/764,391 was filed on January 23, 2004.

The combination of Bongiorno and Lichter does not form the basis for a valid rejection of claim 6 under § 103(a) because neither Bongiorno nor the Lichter provisional application 60/482,557 teaches either (i) coupling one clock circuit after decoupling another clock circuit, or (ii) powering up a clock circuit. Reconsideration of the § 103(a) rejection and allowance of claim 6 are requested.

III. Dependent claim 8

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Bongiorno in view of Chen et al. (U.S. Pat. 6,816,979 B1) (Office Action, p. 10, lines 3-5). The combination of Bongiorno and Chen does not form the basis for a valid rejection of claim 8 under § 103(a) because the combination of Bongiorno and Chen does not teach all of the limitations of base claim 1.

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application under 35 U.S.C. 119(e) is the filing date of the provisional application with certain exceptions if the provisional application(s) properly supports the subject matter relied upon to make the rejection in compliance with 35 U.S.C. 112, first paragraph. See MPEP § 706.02(f)(1), examples 5 to 9." (MPEP 2136.03 III) (emphasis added)

Claim 8 includes the following limitation of base claim 1: "(d) enabling a third clock circuit after the coupling in (c)". Bongiorno does not teach enabling a clock circuit as explained above with regard to claim 1. Chen also does not teach enabling or turning on a clock circuit.

In addition to the limitations of base claim 1, claim 8 recites "disabling a failure detection circuit that performed the detecting in (a)". In the Office action dated December 27, 2006, the Examiner states, "Neither Bongiorno nor Lichter teach disabling a detection circuit" (12/27/06 Office Action, p. 12, line 17). In the Office Action, the Examiner states that "Chen teaches a clock detection circuit wherein the clock detector can be disabled (column 4, lines 38-51)" (Office Action, p. 10, lines 6-8) (emphasis added). The Examiner has not, however, established a *prima facie* case of obviousness because the Examiner has not stated that Chen teaches "a failure detection circuit". Neither claim 1 nor claim 8 recites "a clock detection circuit". The passage of Chen cited by the Examiner teaches a "fast clock detect logic 122" that detects a faster clock as opposed to a failed clock. The cited passage teaches the detection of a faster clock: "The circuit 100 may provide automatic detection and configuration of FIFOs to device blocks to a faster clock." (Chen, col. 4, lines 45-47). Thus, Chen does not teach disabling a failure detection circuit.

Because the combination of Bongiorno and Chen teaches neither enabling a clock circuit nor disabling a failure detection circuit, reconsideration of the § 103(a) rejection and allowance of claim 8 are requested.

IV. Dependent claim 20

Claim 20 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Bongiorno in view of Triece (U.S. Pat. Pub. 2003/0079152 A1) (Office Action, p. 10, lines 15-17). The combination of Bongiorno and Triece does not form the basis for a valid rejection of claim 20 under § 103(a) because (i) the combination of Bongiorno and Triece does not teach turning on a clock circuit, (ii) the combination of Bongiorno and Triece does not teach coupling a system clock

input lead to ground between switching from a current clock to a new clock, and (iii) there is not sufficient motivation to combine the reference teachings.

Claim 20 includes the following limitation of base claim 19: "wherein the means turns on the third clock circuit upon detecting that the first clock signal is inadequate" (emphasis added). Bongiorno does not teach a means for turning on a clock circuit as explained above with regard to claim 19. Triece also does not teach a means for turning on a clock circuit.

In addition to the limitations of base claim 19, claim 20 recites, "the means couples the system clock input lead to ground after decoupling the terminal from the system clock input lead and before coupling the second clock circuit to the system clock input lead". Neither Bongiorno nor Triece teaches coupling a system clock input lead to ground after decoupling from the system clock input lead from a first clock circuit and before coupling the system clock input lead to a second clock circuit.

In fact, Triece teaches against coupling a system clock input lead to ground between switching from a current clock to a new clock. Instead, Triece teaches waiting to switch from a current clock to a new clock until both the current and new clocks happen to be at a logical "0". Note that Triece distinguishes coupling an input to ground from waiting until a clock signal is at a logical "0". Triece explains:

> "[0044] . . . The low power mode which preserves most energy is called the SLEEP mode . . .. In this mode, select switch 258 is turned to position 1 and select switch 330 is turned to position 0, thus cutting off the supply of any clock signal by coupling the respective inputs of ground.
> [0045] The switching process from one clock signal to another clock signal might need synchronization to prevent an undefined status for the central processing unit. To this end, FIG. 3B shows a suitable circuitry to synchronize the switching. . . . Thus, switching can only take place when bot [sic] clocks, the current and the new selected one, are both at a logical "0" and will be therefore synchronized." (Triece, paragraphs [0044]-[0045]) (emphasis added)

In addition, base claim 19 recites, "the means decouples the terminal from the system clock input lead and couples the second clock circuit to the system clock input lead without receiving any signal from the processor" (emphasis added). Thus, the means couples the system clock input lead to ground between switching from a current clock to a new clock without receiving any signal from the processor. Triece also teaches against switching from a current clock to a new clock without receiving any signal from the processor. In Triece, "the central processing unit 100 controls select units 150 and 160 to select one of the four input clocks for distribution to the central processing unit and the peripheral units, respectively" (Triece, paragraph [0032]). "Central processing unit 100 generates a control signal which is sent to synchronizer and control unit 257" (Triece, paragraph [0035]). "Whenever the central processing unit 100 is turned off by selection of the ground signal as a system clock signal, no further transition can take place as the central processing unit 100 cannot execute any instruction. Thus only a reset or a wake-up signal, for example, from watchdog timer 105 can restart the central processing unit 100" (Triece, paragraph [0057]).

Because Triece teaches against both (i) coupling a system clock input lead to ground between switching from a current clock to a new clock, and (ii) switching from a current clock to a new clock without receiving any signal from the processor, there would be no motivation to combine Triece with Bongiorno to arrive at the invention of claim 20.

Reconsideration of the § 103(a) rejection and allowance of claim 20 are requested.

V. Conclusion

In view of the foregoing remarks, Applicants respectfully submit that the entire application (claims 1-23 are pending) is in condition for allowance. Applicants respectfully request that a timely Notice of Allowance be issued in this case. If the Examiner would like to discuss any aspect of this application, the

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Examiner is requested to contact the undersigned at (925) 550-5067.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

By _____
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